WHAT IS CLAIMED IS:

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1. A high-frequency semiconductor device comprising a Si MOS transistor and a lateral polysilicon diode both formed on a substrate,

wherein the lateral polysilicon diode connects a high-frequency I/O signal line and externally supplied voltage VDD, and forward direction of the lateral polysilicon diode is direction from the high-frequency I/O signal line to the externally supplied voltage VDD.

2. A high-frequency semiconductor device of Claim 1, further comprising a lateral polysilicon diode on the substrate, wherein the lateral polysilicon diode connects ground GND and a high-frequency I/O signal line, and forward direction of the lateral polysilicon diode is direction from ground GND to the high-frequency I/O signal line.

3. A high-frequency semiconductor device of Claim 2, wherein lateral polysilicon diodes to the number of "m" are connected between the high-frequency I/O signal line and externally supplied voltage VDD in series, lateral polysilicon diodes to the number of "n" are connected between ground GND and the high-frequency I/O signal line in series, and with assuming the voltage of VDD as V_{dd}, $V_{dd}/(n+m)$ is smaller than 1.1 (V).

4. A high-frequency semiconductor device of Claim 1,

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wherein a lateral polysilicon diode is not connected to a signal line other than a high frequency I/O signal line.

5. A high-frequency semiconductor device of Claim 1 further comprising a capacitor having a lower electrode and an upper electrode both formed with polysilicon, wherein the lateral polysilicon diode and the lower electrode of the capacitor are formed from same polysilicon layer, and gate electrode of the MOS transistor is formed from another polysilicon layer.

6. A high-frequency semiconductor device of Claim 1 further comprising a capacitor having a lower electrode and an upper electrode both formed with polysilicon, wherein the lateral polysilicon diode and the lower electrode of the capacitor are formed from same polysilicon layer, and gate electrode of the MOS transistor and the upper electrode of the capacitor are formed from another polysilicon layer.

7. A high-frequency semiconductor device of claim 5, wherein polysilicon layer to form the upper electrode of the capacitor is also left on and covering PN junction of the lateral polysilicon diode.

8. A high-frequency semiconductor device of claim 5, wherein a dielectric layer to form the capacitor is also left on and covering PN junction of the lateral polysilicon diode.

9. A manufacturing method of high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes and a capacitor on a substrate, and the lateral polysilicon diode

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connects a high-frequency I/O signal line and externally supplied voltage VDD, and the other lateral polysilicon diode connects ground GND and the high-frequency I/O signal line;

wherein the lower electrode of the capacitor and the lateral polysilicon diode are formed from a first polysilicon layer,

the insulating film of the capacitor is formed from a first dielectric layer,

the upper electrode of the capacitor is formed from a second polysilicon layer,

the first dielectric layer is also left on a certain region of the first polysilicon layer at which PN junction of the lateral polysilicon diode is to be formed,

and an edge of a resist mask used for injecting ion into N-type region of the lateral polysilicon diode and an edge of a resist mask used for injecting ion into the P-type region of the lateral polysilicon diode are placed on the first dielectric layer being left.

10. A manufacturing method of high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes and a capacitor on a substrate, and the lateral polysilicon diode connects a high-frequency I/O signal line and externally supplied voltage VDD, and the other lateral polysilicon diode connects ground GND and the high-frequency I/O signal line,

wherein the lower electrode of the capacitor and the lateral polysilicon diode are formed from a first polysilicon layer,

the insulating film of the capacitor is formed from a first dielectric layer,

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the upper electrode of the capacitor is formed from a second polysilicon layer,

the second polysilicon layer is also left on a certain region of the first polysilicon layer at which PN junction of the lateral polysilicon diode is to be formed,

and an edge of a resist mask used for injecting ion into N-type region of the lateral polysilicon diode and an edge of a resist mask used for injecting ion into the P-type region of the lateral polysilicon diode are placed on the second polysilicon layer being left.

11. A manufacturing method of claim 9, wherein gate electrode of the MOS transistor is formed from the second polysilicon layer.

12. A high-frequency semiconductor device of claim 1 further comprising a clamp circuit connected between the externally supplied voltage VDD and ground GND, wherein the clamp circuit operates to flow current within voltage lower than the absolute value of reverse bias breakdown voltage of the lateral polysilicon diode.